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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
09/397,952	09/17/99	AHMAD	A	MICRON.061DV

020995 MMC1/0802
KNOBBE MARTENS OLSON & BEAR LLP
620 NEWPORT CENTER DRIVE
SIXTEENTH FLOOR
NEWPORT BEACH CA 92660

EXAMINER	
RAO, S	
ART UNIT	**PAPER NUMBER**
2814	4

DATE MAILED: 08/02/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary

Application No.	Applicant(s)
09/379,952	Ahmad, Aftab
Examiner	**Group Art Unit**
S.H. Rao	2814

☒ Responsive to communication(s) filed on *Dec 28, 1999*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-15 and 23-28* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-15 and 23-28* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *3*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Specification

1. The attempt to incorporate subject matter into this application by reference to U.S. Serial No.08/871,210 is improper because if this application has matured into a patent the phrase ," now Patent no . 6,037,639" should be included in the first line of the specification. Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahmad et al (U.S. Patent No. 5,405,791, herein after Ahmad).

With respect to claim 1 Ahmad, teaches a process for forming a gate structure on a semiconductor substrate including the steps of : semiconductor substrate(13) with channel region, source/drain regions (Ahmad fig. 5A 13,52,), gate dielectric-oxide (23), and conductive

layer (polysilicon layer 17), forming insulator element region and transforming it into a side wall spacer. (Ahmad figs. 2-4).

With respect to claims 2-7 Ahmad teaches a process for forming a gate structure on a semiconductor substrate including the steps of :

wherein the insulator forming step includes a doping step (31, col.4 lines 3-9 and fig. 3), insulator element region includes silicon and insulator material (31 is made of TEOS oxide having silicon and oxide), it is well known in the art to substitute nitrogen for oxygen and doping at a given rate in insulating material (See Col. 3 lines 50-54). Oxidizing the conductive layer (21, Col.3 lines 53-55), polysilicon and bird's beak extending into the conductive layer (Col. 3 lines 57-60 and fig. 2).

With respect to claims 9,10 forming a nitride layer on the substrate , wherein the nitride layer extends under the conductive layer (41).

With respect to claim 11 , Ahmad at col. 3 lines 11-15 teaches silicon oxide spacers.

With respect to claim 12 , Ahmad at col. 4 lines 51-55 and fig. 7 teaches depositing a second sidewall spacer over the first side wall spacer.

With respect to claim 13 it repeats the steps of claim 1 and furthermore recites the formation of an oxide layer from the conductive layer and a protective layer with higher dielectric constant. (see layer 21, col. 3lines 53-55) and forming nitride protective layer (41). It is well known in the art that nitride has higher dielectric constant than oxide.

With respect to claim 14, it repeats the steps of claims 8 and 10: Claim 15 repeats the steps of claims 1,4 and12; Claim 23 repeats the steps of claims 14 and 15 and the above discussion is incorporated here by reference.

With respect to claims 24- 28 , Ahmad at col. 4 lines 5-9 teaches using an ozone (oxygen) atmosphere, col.4 lines 33-35 teaches a boron implant, and figs . 8-10 teach a graded junction between the channel and S/D regions.

The prior art made of record that is deemed relevant to the instant disclosure , but not applied in this office action are U.S. Patent Nos. 5,895,955 (Gardner et al.) And 6,030,875 (May et al.).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The fax number is (703) 308-7722 or -7724.The Examiner can be normally reached on Monday-Friday from 9.30 a.m. to 6.00 p.m. (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor Ex. Olik Chaudhuri, can be reached at (703) 306-2794.

9. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission at the above mentioned fax numbers.

10. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology center 2800 receptionist at (703) 308-0956.

March 22, 2000

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800